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Practical Analysis of Backplane Vias

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Abstract

Accurate, verified models for vias in a multilayer circuit board are necessary to predict link performance in the GHz regime. This paper describes the methodology of using measurements on a test vehicle to build a high bandwidth, scalable model of long vias which includes the through and stub effects which can be used for system simulation. This simple model also provides valuable insight into the root cause of performance limits and how to overcome them.

Author(s) Biography

Eric Bogatin received his BS in physics from MIT and MS and PhD in physics from the University of Arizona in Tucson. He has held senior engineering and management positions at Bell Labs, Raychem, Sun Microsystems, Ansoft and Interconnect Devices. Eric has written 4 books on signal integrity and interconnect design and over 200 papers. His latest book, Signal Integrity- Simplified, was published in 2004 by Prentice Hall. He has taught over 4,000 engineers in the last 20 years. Many of his papers and columns are posted on the www.BeTheSignal.com web site.

Lambert (Bert) Simonovich graduated in 1976 from Mohawk College of Applied Arts and Technology in Hamilton, Ontario, Canada as an Electronic Engineering Technologist. Over his 32 year career at Nortel, he has helped pioneer several advanced technology solutions into products and has held a variety of R&D positions, eventually specializing in backplane design over the last 25 years. Besides his current role as backplane architect for new high speed designs, he is engaged in signal integrity, characterization and modeling of high speed serial links associated with backplane interconnects. He holds two patents and one IEEE publication.

Sanjeev Gupta, the Signal Integrity Applications Expert in the EEsof EDA Division of Agilent Technologies, has over eighteen years of experience in high frequency design and simulation. Before joining Hewlett Packard, he worked as a high frequency design engineer/scientist at the Defense Research and Development Organization in India. His background includes the design and development of 100 MHz to 100 GHz active and passive circuits for a wide variety of applications. His most recent activity is focused on influencing the Signal Integrity Design Flow in ADS. He received a Master's Degree in Microwave Engineering from the University of Delhi, India in 1988. Sanjeev was awarded the Hewlett Packard President's Award in 1998 for his contributions to the company.

Mike Resso is the Signal Integrity Measurement Specialist in the Component Test Division of Agilent Technologies and has over twenty-five years of experience in the test and measurement industry. His background includes the design and development of electro-optic test instrumentation for aerospace and commercial applications. His most recent activity has focused on the complete multiport characterization of high speed digital interconnects using Time Domain Reflectometry and Vector Network Analysis. He has authored over 30 professional publications including a book on signal integrity. Mike has been awarded one US patent and has twice received the Agilent "Spark of Insight" Award for his contribution to the company. He received a Bachelor of Science degree in Electrical and Computer Engineering from University of California.

Introduction

It is well established that often, the largest impedance discontinuity in a high speed serial interconnect is from the vias used when the signal changes layers. Signal vias are typically placed anywhere in a design to optimize routing density and especially at connectors. These vias can be a dominate source of degradation of the eye diagram.

The measured differential insertion loss of two different differential vias in a 26 layer board is shown in Figure 1. In addition, a cross section of the vias is shown to illustrate the two important features of a through hole via: the through path and the residual stub.

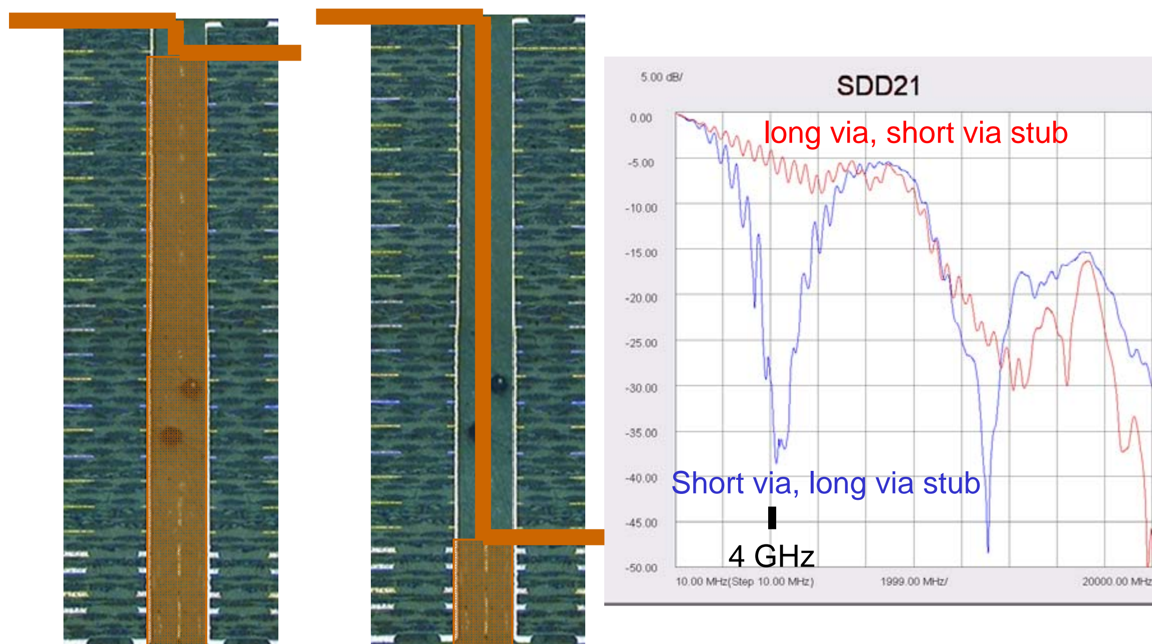


Figure 1. Cross section of two through hole vias, one with a long stub (left) and one with a short stub (right), with their measured differential insertion loss.

The presence of the via stub causes resonances in the differential insertion loss, which can significantly detract from the insertion loss if the via stub is very short. While stub lengths can be minimized, they can never be completely eliminated. In order to evaluate the impact of an arbitrary length via stub and the impact of the through part of the via on performance, a scalable model which accurately accounts for these effects is essential. Such a model can be used to explore design space and balance design tradeoffs.

Using a well characterized test vehicle and accurate 4-port measurements, the "inverse scattering" technique can be used to create a scalable circuit topology, extract parameter values for the model and verify its bandwidth. This model can then be used to "hack into" the via design, identifying the sources of limitations and how they can be overcome.

Inverse scattering is the technique of using measured data as a target value and adjusting parameters in the model until the simulated response of the model closely matches the measured response of the physical interconnect. The agreement between measured and simulated performance is an indication of the possibility the model is a good electrical representation of the real physical structure. It can then be used to explore the root cause of performance effects and design optimizations.

In this project the measurements were taken with an Agilent N5230A VNA. The initial evaluation of the data was done with Agilent's Physical Layer Test System (PLTS) software and the model fitting, simulation and analysis were performed with Agilent's Advanced Design System (ADS) software.

Test Vehicle

A 26 layer board was fabricated with pairs of differential signal vias and adjacent return vias. It was designed to evaluate the signal path from the top layer, through a via to a buried signal layer, down a uniform stripline differential pair to another via, and then back up to the top surface. A close up of the top of the board is shown in Figure 2.

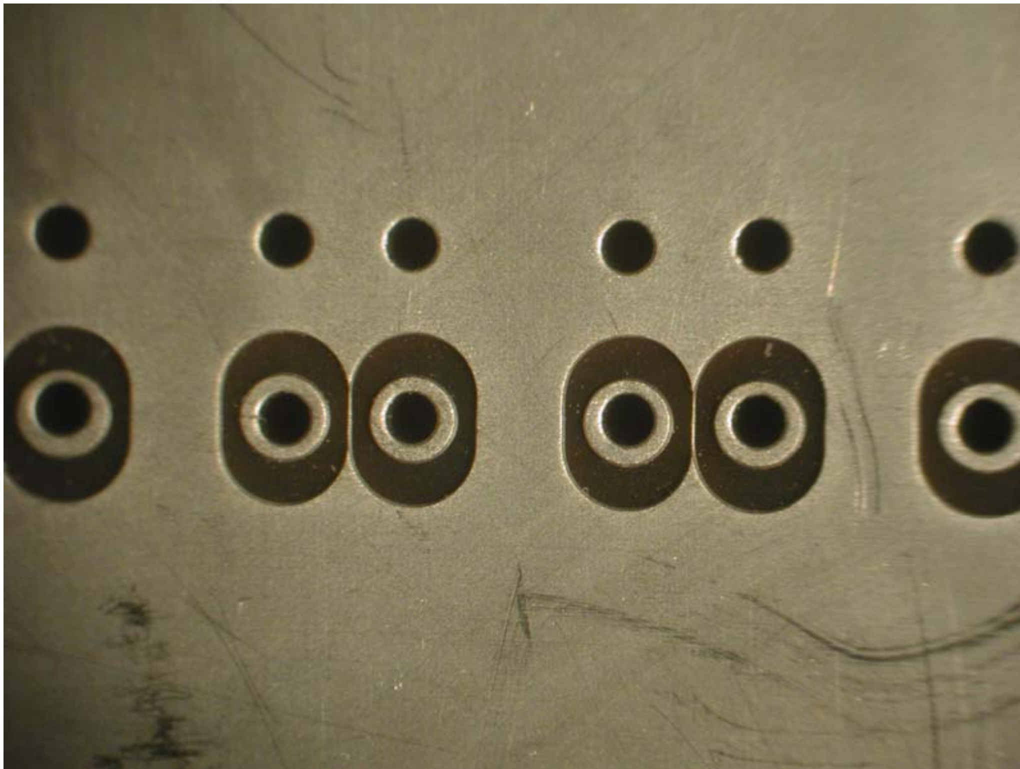


Figure 2. Close up of the differential via launch pads of the test vehicle and adjacent return vias.

This test board was designed with via pairs transitioning to every signal layer. A representative set of three via pairs was selected to build the model with signals on layers

2, 10 and 20. The resulting stub lengths were approximately 270 mils, 178 mils and 64 mils long. This is summarized in Figure 3.

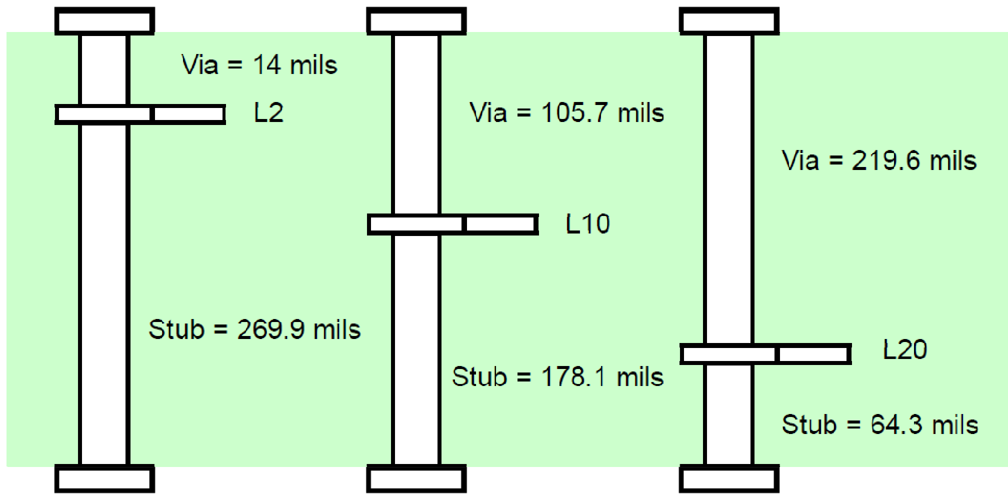


Figure 3. Cross section of the three vias selected to base the scalable model showing the section of through via length and the residual via stub length.

The connections between the entry and exit vias are by uniform, tightly coupled, stripline differential pairs. On their far end, an identical via pair brings the differential signal back up to the surface where the second probe pair makes contact. The uniform stripline path is approximately 6 inches long. This is diagramed in Figure 4.

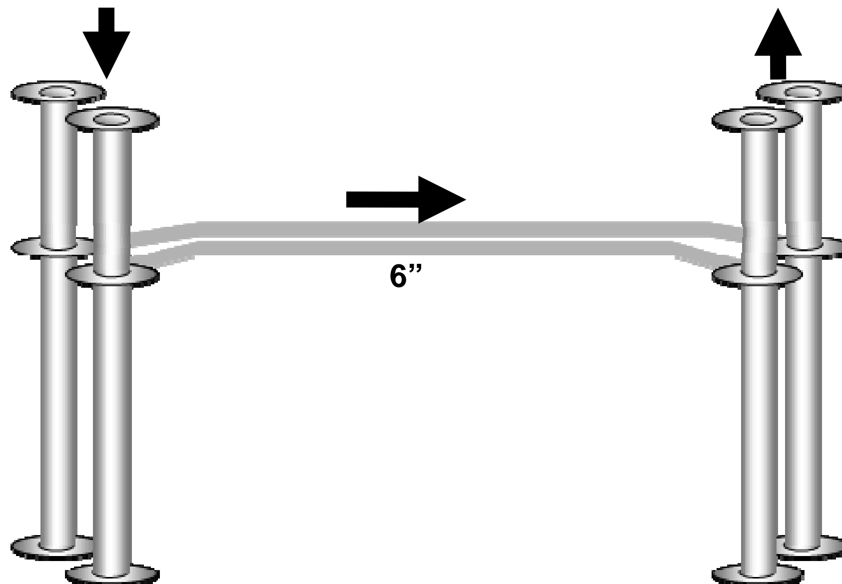


Figure 4. Illustration of the topology of each test structure from the top contact, through via, stripline interconnect and final via.

A simple, custom designed probe was built to interface between the coax connections of the VNA to the signal pads of the test vehicle. This was built from pieces of semi-rigid coax with the tips exposed to contact the surface of the board. A close up is shown in Figure 5.

Figure 5. Close up of the custom, differential, semi-rigid coax probe tip.

An Agilent N5230A VNA was used to perform 4-port, single ended S-parameter measurements on each of the three signal paths. The VNA was calibrated at the end of the coax cable; this means that the custom semi-rigid coax probe tips were part of the measurement. The circuit topology model used to interpret the results must include a model for the probe tips.

An example of the measured differential return loss of the path with the longest via stub, displayed in the time domain as the differential TDR response is shown in Figure 6.

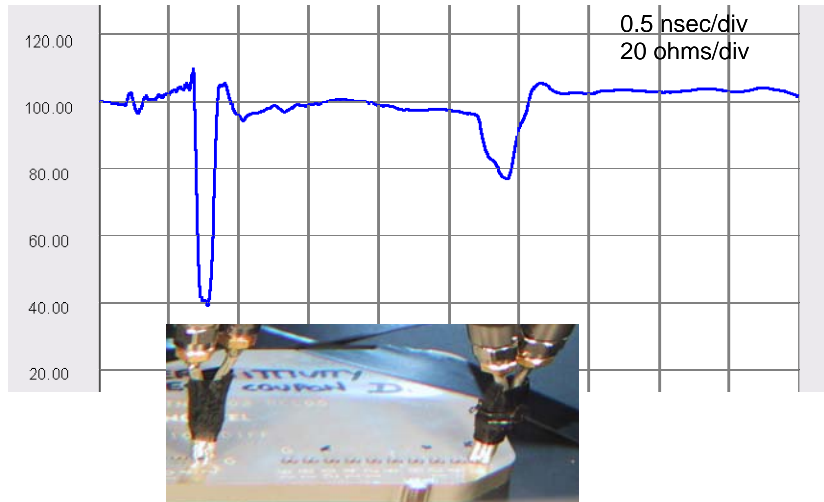


Figure 6. Measured differential TDR response, with differential impedance as the vertical scale, for the signal path with the longest via stub.

This measured response shows the impact of the probe fixture, the first via connection, the uniform stripline path to the second via, and the impact of the second via. Of course, the rise time degradation through the 6 inches of signal trace causes the second via to look different than the first via, even though they are identical. Any good model of the signal path will automatically take this effect into account.

Measurement Analysis

A 4-port measurement contains a huge amount of information. Any single domain has 10 unique S-parameter values. In the frequency domain, each of these is really two terms, a magnitude and phase. This is 20 unique plots.

The basic measurement for each differential pair test line is the collection of 4-port single ended S-parameters. An example of the measured response for the long via stub test line is shown in Figure 7.

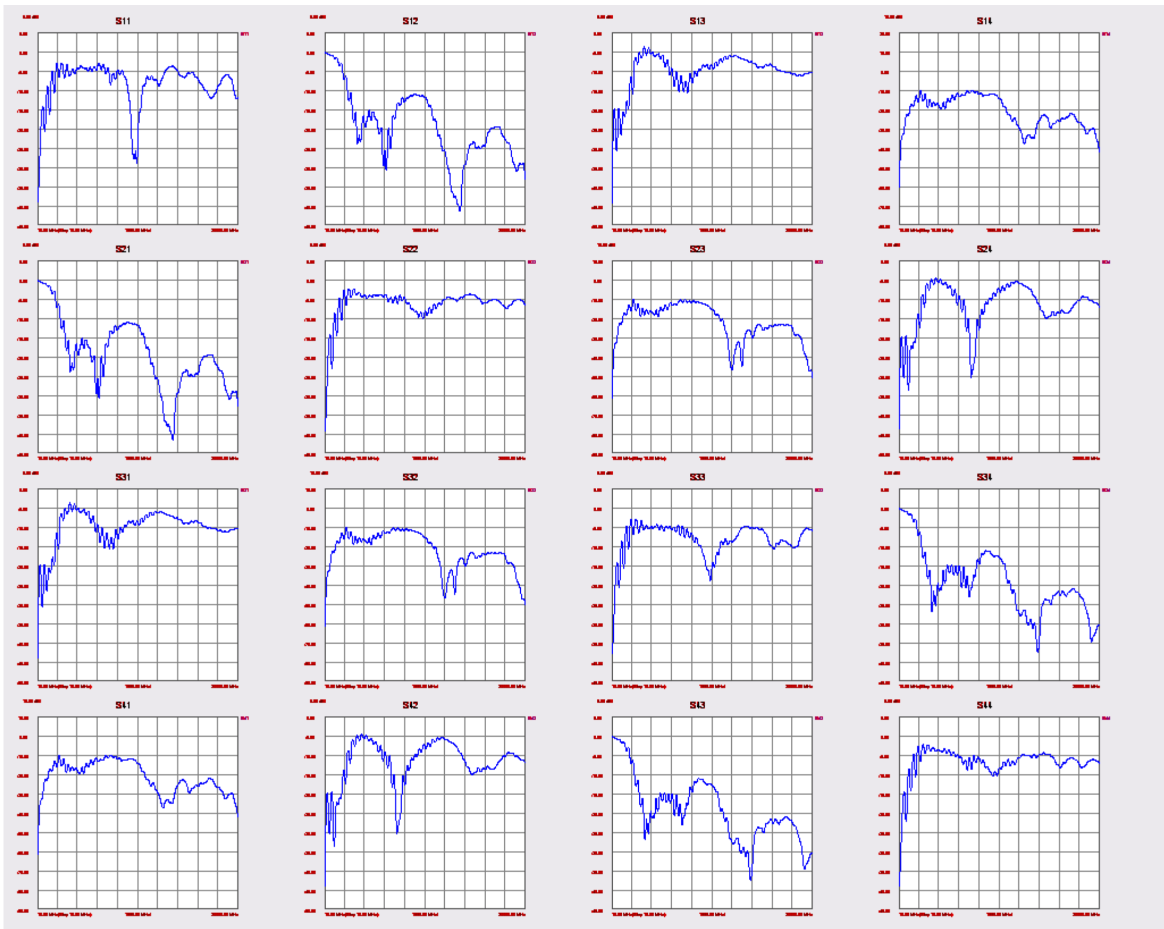


Figure 7. Example of the measured 4-port single ended S-parameters for the test structure with the longest via stub, displayed using Agilent PLTS. Not shown are the phase plots for each S-parameter.

These single ended, frequency domain measurements can be reformatted to be displayed as differential, frequency domain plots or as single ended or differential time domain plots with either step or impulse response.

All together, there are four different domain formats, each having two sets of plots for 10 different unique data sets. This is a total of 4 x 2 x 10 = 80 different possible plots for each of the three different test lines, or 240 different plots of data to evaluate. This is a huge amount of data to review and keep track of. For this reason, Agilent PLTS was used to mine the important information from this data set.

The first question to address in any measured data set is how symmetric are the structures. This applies to the line to line symmetry and the symmetry from one end to the other. The single ended return loss from each of the four ports of the long stub structure is shown in Figure 8.

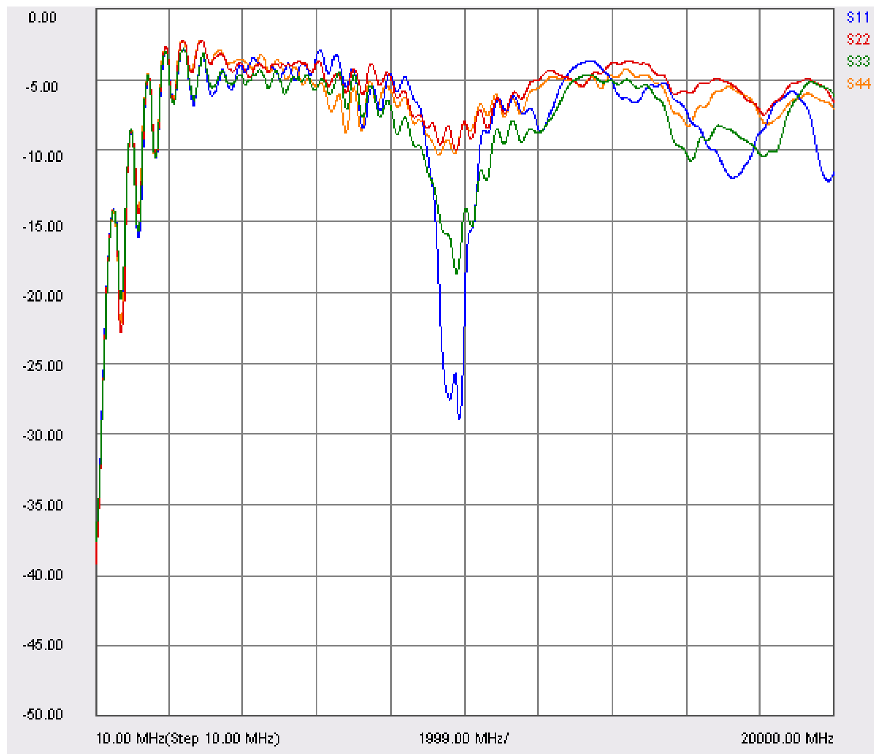


Figure 8. Single ended return loss from each of the four ports of the long via stub measurement.

Nominally, each of these measurements should be identical for a symmetrical test structure. While they effectively overlap each other at frequencies below about 3 GHz, there is considerable difference between them at about 10 GHz and beyond. This suggests that there is something about the combination of the connector and test line that introduces a line to line asymmetry. One clue to this is hinted when looking at the TDR response of the launches, as shown in Figure 9.

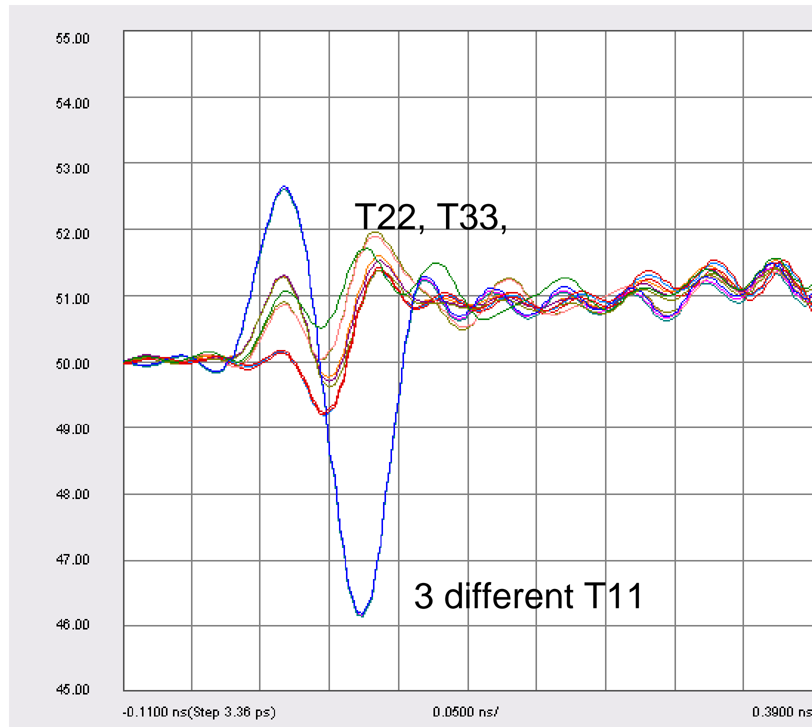


Figure 9. Close up of the single ended TDR response of each of the four ports and each of the three test lines for a total of 12 different launches.

From this measurement of the 12 different launches, it is clear that the fixture in channel 1 is very different from the behavior of the launches of the other channels, and they are each slightly different from each other as well.

The ringing behavior has a period of about 100 psec, which corresponds to a frequency of about 10 GHz. This suggests that the large dip in the return loss at 10 GHz is due to the asymmetry in the fixture launches. To account for this effect, the launches have to be uniquely modeled.

Building a Simple Scalable, Topology Based Model

There are two generic kinds of models: behavioral models and circuit topology models. S-parameters are called behavioral models because they can be used in a system simulation without any assumptions about the structure they came from. They describe the behavior of the structure to incident waveforms from calibrated port to calibrated port. Once the device is measured, the S-parameters can be used as a behavioral representation of the actual structure.

A limitation to any behavioral model is that the S-parameters represent everything connected between the calibrated reference planes of the VNA. In this case, the measured behavioral model includes the semi-rigid custom probes. Elaborate de-embedding and calibration schemes have been devised to remove fixture effects from the measurement to leave behind in the S-parameters, just the structure of interest.

A circuit topology model is a circuit diagram or schematic representation of the structure which, when run in a circuit simulator, predicts any measureable performance of the structure. For any physical structure, there is no one unique circuit topology that describes it. Rather, many different circuit topologies can give the same performance, up to some bandwidth.

Our goal is to create a circuit topology that is simple, yet matches the measured performance up to a high bandwidth. To provide the most benefit, the topology model should have features in it that can be directly related to physical features of the structure. Further, these features should be parameterized so that the impact on the simulated electrical performance can be investigated when a specific design parameter is varied. In this way design space can be explored.

For this special test structure, a topology based model should have elements that take into account the custom probe launch, the differential via, which includes the through part and the stub part, and the uniform stripline section. The simplest topology that includes these features is shown in Figure 10.

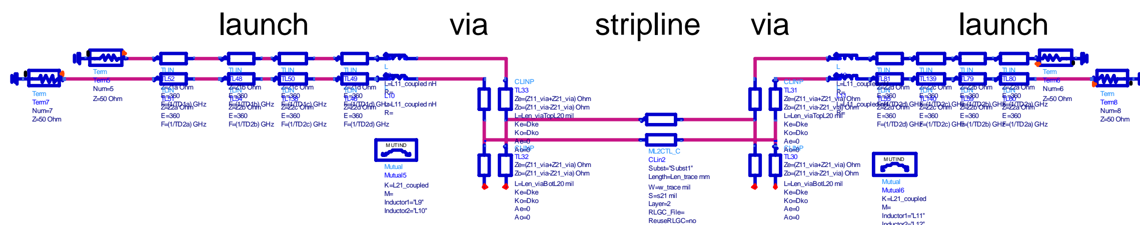


Figure 10. Simple topology based circuit model for the complete structure as constructed in Agilent ADS software.

The goal is to use the measured performance of the structure as a target and adjust the parameters of the circuit model so the simulated S-parameters of the model match the measured response. The only way to know if this is a reasonable circuit topology is to see if a set of reasonable parameters can be found to give good agreement between the measured and simulated S-parameters. If the measured performance can be accurately predicted by the model, then there is confidence this model is a good representation of the actual physical structure.

However, if good agreement can't be found, it may be because there is a key element in the real structure that is not taken into account in the simplified model, or it could also be that we were not efficient enough at exploring all parameter values to find the best set of values. There is no guarantee of success when starting out with a circuit topology. The only way of establishing confidence in a specific topology is by being successful in matching it to the measurement. This is another example of the old line, "the proof is in the pudding."

Each probe launch is composed of four, uniform transmission line elements. These are individually optimized for the launch on port 1 and then for the other three ports, to take

into account the asymmetry between them. The cross talk at the tips due to the return current common to the tips is accounted for by the mutual inductor element at the end of each probe. In this case, the launches on ports 2, 3, and 4 are made identical in the model.

By measuring the 4-port response of the launches, when open and when shorted to a plane, the characteristic impedance and time delay of each of the four different transmission line elements and the mutual inductance term, a total of 10 different parameters, were fit to ports 1 and ports 2, 3, and 4. The final agreement with the measured response is shown in Figure 11.

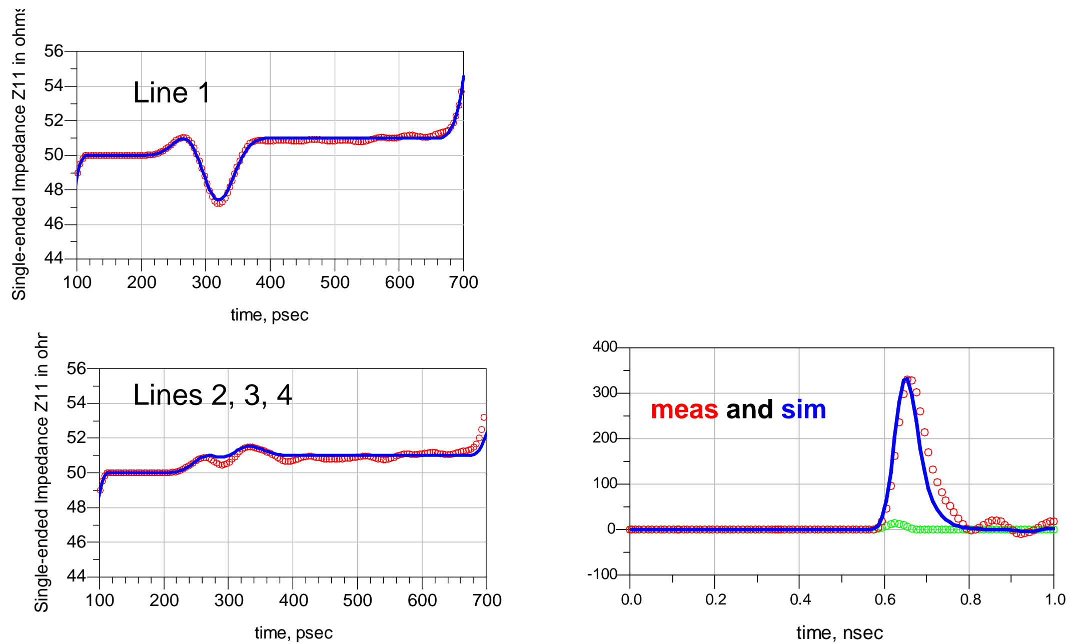


Figure 11. Comparison of the measured and simulated single ended TDR response of the four probe tips when connected to a shorting plane.

The via model is the simplest possible model. It consists of a uniform, lossless differential pair with two segments. The top segment is the through via connection path, while the bottom segment is the residual via stub. There are six parameters that define all the elements of this model:

- Odd mode impedance of the differential pair
- Even mode impedance of the differential pair
- Odd mode dielectric constant
- Even mode dielectric constant
- Top length of thru via connection
- Bottom length of via stub

To further simplify the model, the odd and even mode dielectric constants are assumed to be the same, which we label as Dk-xy. This is the effective dielectric constant for electric field lines in the xy plane of the board- in the plane of the glass weave of the laminate.

The lengths of the top and bottom segments of the via were taken directly from the design of the board, so these are not parameters to adjust. This reduces the number of parameters to fit to the measured response to three: the odd and even mode impedances and the effective dielectric constant the signal sees while in the via.

The uniform stripline structure is modeled as a simple, dual stripline based on the geometry. Agilent's ADS tool has a built in 2D field solver. It can convert the cross section geometry information and dielectric constant values into the circuit topology based on a matrix representation of the line parameters. This includes losses as well.

The cross section of the stripline section is defined in terms of the dielectric thicknesses, line width, thickness of the trace and dielectric constants of the laminate. A cross section of the actual board is shown in Figure 12.

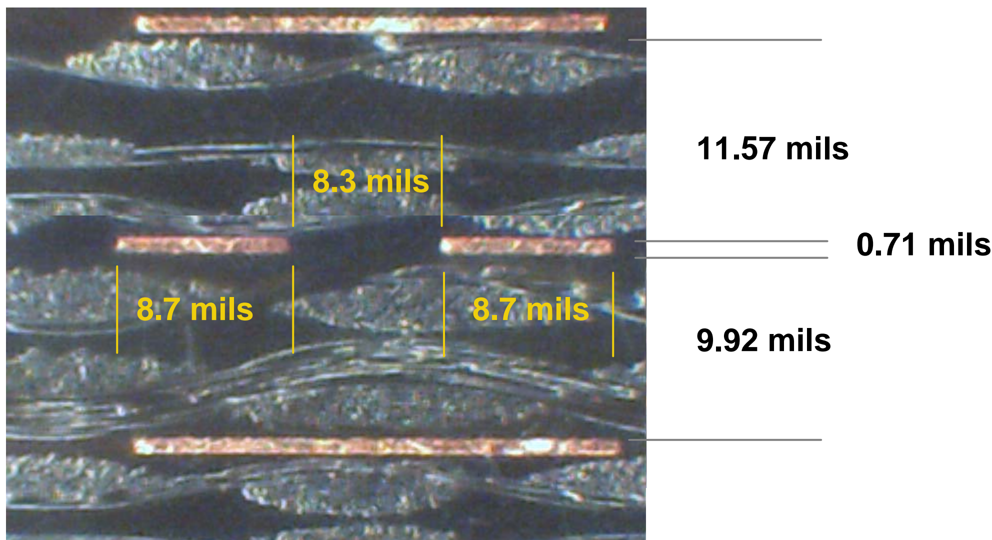


Figure 12. Cross section of the uniform stripline region of the interconnect.

Each of these dimensions was input into the ADS multilayer interconnect library (MIL) model for the stripline, with no parameter fitting. In addition, the laminate properties of the pre-preg layer (top) and the core layer (bottom) were well known from the manufacturers' data sheet, based on the precise composition of the type of glass and number of layers in each section.

The manufacturer's values of the dielectric constant of the pre-preg and core layers were 3.58 and 3.69. These values were used in the model with no adjustment. However, the value of the dissipation factor given by the manufacturer is about 0.008. It has been the experience of some of us that in general the manufacturer's values of dissipation factor for modified FR4 type materials are never this low, but closer to 0.02. In this model, the value of 0.02 was used.

For this entire model, there were only three parameters to fit from the measured data, the odd mode impedance of the differential pair, the even mode impedance of the differential pair and the effective dielectric constant the signal sees while inside the via.

Dielectric Constant

When a signal propagates in a stripline through a fiberglass reinforced laminate, the electric field is in the z-direction, normal to the surface of the board. It is affected by the relative amount of glass material, resin content, and their distributions. As the resin has a typical dielectric constant on the order of 3 and the glass has a dielectric constant on the order of 6, the effective, composite dielectric constant is between 3.5 and 4.5, depending on the relative amount of glass and resin.

A laminate supplier able to reproducibly manufacture laminate layers can provide reproducible and accurate values of the dielectric constant of each layer, given the type of glass weave, the type of resin, the number of layers of glass weave and the total layer thickness.

However, this is not the same dielectric constant the signal would see when it propagates through a via. In this path, the electric field is between the barrels of the via and lies in the x-y plane. The electric field sees a different combination of glass weave and resin content, with different distributions. This is illustrated in Figure 13.

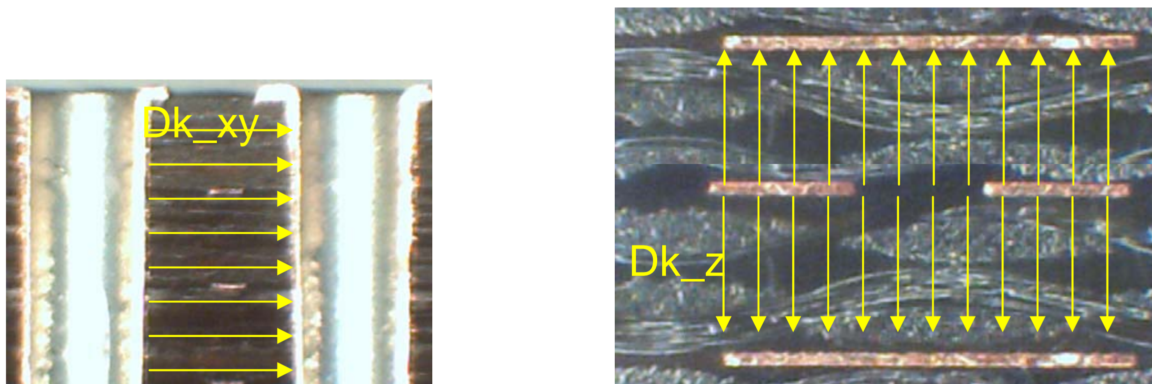


Figure 13. Electric field direction in the laminate in the two different regions, between via barrels (left) and in the stripline interconnect (right).

Does the signal see the same relative dielectric constant in both directions of this non-homogeneous dielectric constant material? It is well established that the effective dielectric constant in the x-y direction is typically higher than in the z direction making the dielectric material anisotropic in nature. Though the dielectric constant may be about 3.7 in the z- direction, it will generally be higher in the x-y direction.

The differential pair model has the effective dielectric constant as a parameter. This one value for each of the three via structures is adjusted to fit the measured response of the

insertion loss, return loss and delay for all three via lengths. Only one value of effective dielectric constant fits all nine conditions simultaneously.

The large dip in the insertion loss of the long stub is a direct result of the quarter wave resonance of the dangling stub. This resonant frequency is a good first order measure of the effective dielectric constant associated with the signal propagating down the stub. From the measured resonant frequency and the stub length, the effective dielectric constant can be estimated using the following equation [3].

$$Dk = \left[\frac{c}{4 * Stub_length * f} \right]^2$$

Where:

c = Speed of light (1.18E10 inches/sec)
Stub_Length in inches
f = ¼ wave frequency in Hz

Using the layer 2 parameters for stub length (270 mils) and resonant frequency (4.3 GHz), the effective Dk = 6.4, which matches the value extracted as the best fit of the parameterized model to all the measured data.

One interpretation of the resonant frequency is that it is due to a higher effective dielectric constant in the via region, due to the in-plane electric field seeing a strong influence from the glass weave.

Another interpretation of the resonant frequency is that the in-plane dielectric constant is actually the same as the z- axis, bulk value, but there is excess distributed capacitance from the fringe fields of the via barrel interacting with the edges of the planes.

Both models would predict a higher effective dielectric constant and lead to the same resonant frequency. The differential pair model is perfectly consistent with both explanations. The only way of distinguishing between these two models is with a 3D field solver, which is part of a follow up study.

Optimized Parameter Values

The differential response is only sensitive to the odd mode impedance and independent of the even mode impedance. When optimizing to the differential S-parameter response, there are only two parameters that need to be fitted, the odd mode impedance and the dielectric constant in the xy plane. Parameter space is simple to explore.

The best set of values that provide good agreement between the differential insertion and return loss and the differential delay, for each of the three different via configurations is

Zodd = 32 ohms
Dk_xy = 6.4

Using these values and the other fixed parameters of the model, the agreement between the measured and simulated S-parameter values is shown in Figure 14.

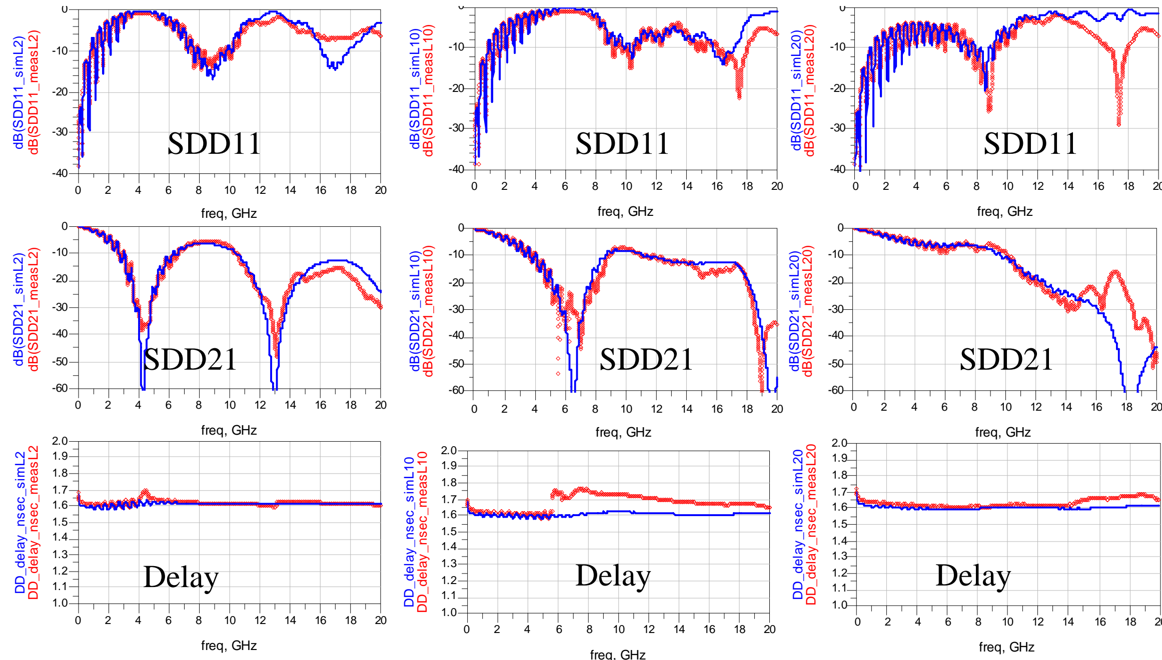
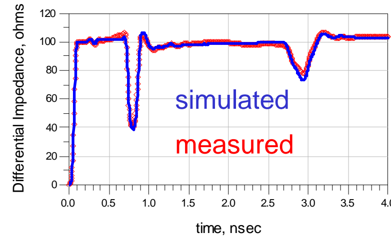


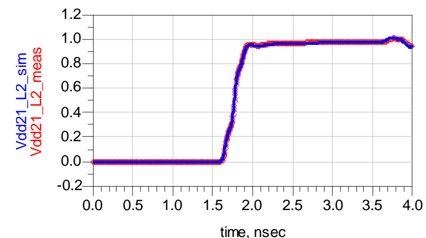
Figure 14. Measured differential response (red circles) and the simulated response of the optimized model (blue line) for the return loss, insertion loss and delay of the long stub, medium length stub and short stub vias, from left to right

The agreement between the measured response and the simulated response using this simple model is seen to be excellent up to a bandwidth of about 14 GHz. This suggests that the simple model of a differential via as a section of uniform differential transmission line is an accurate topology and the values extracted are reasonable values.

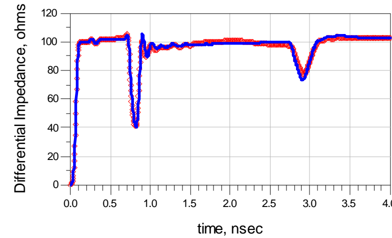
Using these values, the transient performance of the differential reflected and transmitted signals can be compared. The simulated and measured values are shown in Figure 15.

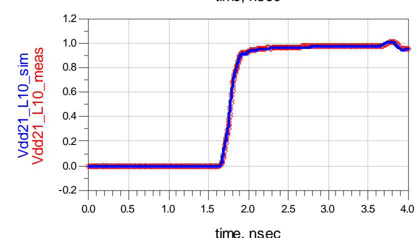
L2: Long Stub



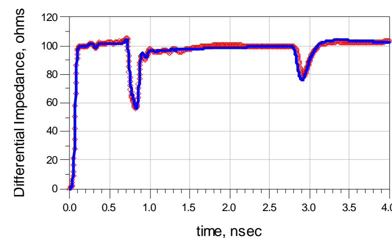


L10: Medium Stub





L20: Short Stub



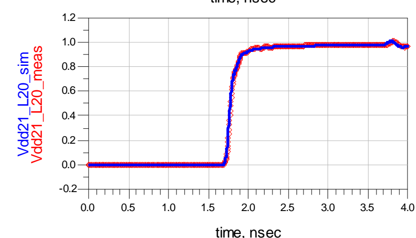


Figure 15. Differential TDR and TDT response of the three different via stub lengths, measured and simulated.

The differential TDR response is a good first order measure of the impedance profile of the 6 inch long stripline interconnect. It is interesting to note that without using any fitting at all, but just the design dimensions and manufacturer supplied dielectric constants [1], the differential impedance of the stripline sections on each layer are accurately predicted to within one ohm. This is evident by looking at the region after the via in the TDR responses.

This suggests that if the cross section geometry and layer stack up construction is well known, differential impedance can be designed to a few percent of the target value. It is also astonishing that so simple a model is able to describe the behavior of this complex structure over such a wide range of via stub lengths, frequency and time domain ranges.

To extract the even mode impedance of the via structure, the common signal's time domain reflection can be used. The reflected common signal is simulated as the even mode impedance of the via differential pair is varied to find the value that best fits the measured response. The result is shown in Figure 16.

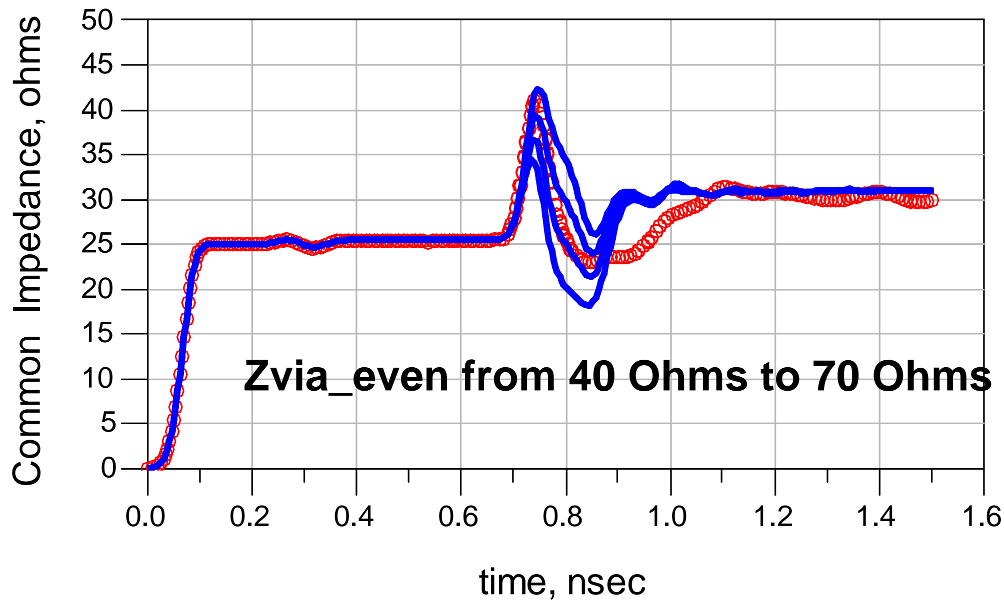


Figure 16. Common signal's time domain reflected response for the long via with short stub, showing the measured response in red circles and the simulated response in blue line, for four different values of even mode impedance.

The best fit is for an even mode impedance of about 60 ohms, though none of the values are such a great match. There are clearly effects in the real via which are not being taken into account in this simple model.

It is remarkable that the differential response is so well described by this simple model yet the common response is not so well described. One possible explanation is that the common signal has some return current coupling through the planes, complicating the performance into something other than a simple uniform differential pair transmission line model.

The differential signal sees the two signal vias tightly coupled together, and only a small fraction of the differential signal's return current is through the adjacent planes or return via. This is the belief of why the behavior of the differential signal matches the behavior of a simple differential pair model so well.

In comparison, the return path for the common signal is mostly through the adjacent return vias and coupling through the planes. While the return vias would look like a uniform transmission line, the impact of the coupling of return current through the planes is not so well described by this model. Some of the return current sees a higher impedance that may be inductive due to the spreading inductance in the planes, and not fit a uniform transmission line model.

This is an area that can only be explored using a 3D EM field solver and is part of the follow on study.

Using the values of the odd mode impedance of the via structure as 32 ohms and the even mode impedance as 60 ohms, the single ended impedance of the via can be estimated as their average, or 46 ohms. These values, extracted from the measurement, are summarized as:

- Zodd = 32 ohms
- Zeven = 60 ohms
- Zo = 46 ohms
- Zdiff = 2 x Zodd = 64 Ohms
- Zcomm = ½ x Zeven = 30 Ohms

From these values, it is clear that the vias behave like a tightly coupled differential pair. This means the two signal vias are tightly coupled to each other and loosely coupled to both the return vias and any return path through the planes.

The value for the effective dielectric constant to match the measured and simulated performance is Dk-xy = 6.4. If a different value were used, such as 3.8, close to the value for the bulk dielectric constant as seen by a signal propagating in the stripline interconnect, the agreement between the measured and simulated results would not be nearly as good. This is illustrated in Figure 17.

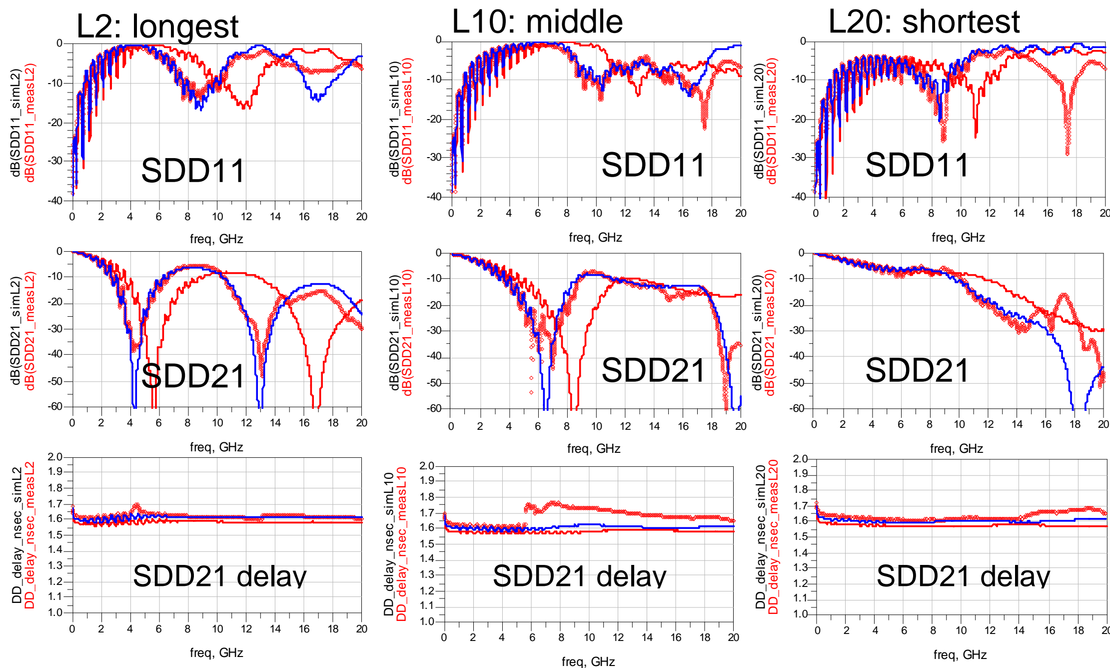


Figure 17. Comparison of the measured (red circles) and simulated performance using a value of Dk-xy of 3.8 and 6.4. The blue line is for a Dk-xy of 6.4, showing good agreement and the red line is for a value of Dk-xy of 3.8, showing much worse agreement.

Exploring Design Space

This parameterized, scalable model for the via can now be used to evaluate the performance in different conditions. The via model is just the differential pair, with two different lengths, the top, through section, and the bottom stub. Any combination of lengths can be simulated and the behavior of just the via evaluated.

For example, the response of just the long through via and 64 mil long via stub can be simulated using the model. Or, this same long through via, with the bottom 64 mil long via stub back drilled away can be evaluated. The comparison of the differential return and insertion loss of these two cases of a long through via, with and without a via stub is shown in Figure 18.

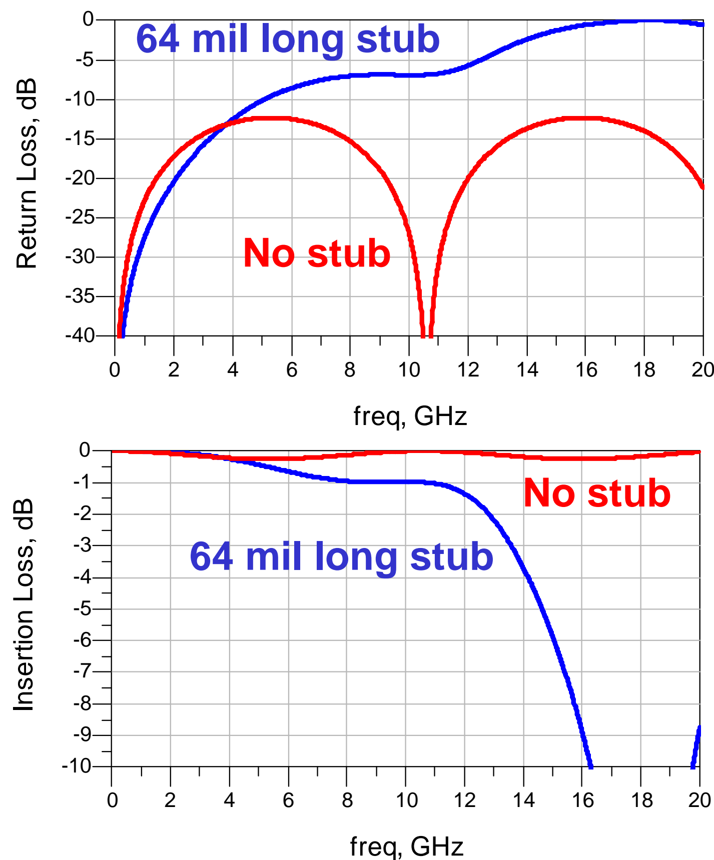


Figure 18. Differential response of the model for the case of the long through via, with and without the residual 64 mil stub.

It is instructive to note that a long via, even with a differential impedance of 64 ohms, far from the 100 ohms of the environment it is in, can look pretty transparent up to frequencies above 20 GHz. The problem with vias is not the through part, but rather it is from the residual via stub.

In comparing the two cases in the above figure, we can see that the impact of this 64 mils long stub begins to show up above 4 GHz, and dominates performance above 8 GHz. Eliminate the stub and the insertion loss is never more than a small fraction of a dB.

By far, the biggest gain in performance is returned by reducing the via stub to as short a length as possible. In this case, the impedance discontinuities would be due to the series impedance of the via.

Estimating Via Impedance

The specific geometry of this via gives it a differential impedance of 64 ohms. It is interesting to compare this extracted value to the value that could be estimated using a simple approximation.

The two signal vias look like a simple pair of round rods. If we assume there is no coupling to the adjacent return vias or into the planes, we could approximate the differential impedance of the pair of vias using the parallel rod approximation. The differential impedance is given by:

$$\text{Zdiff} = \frac{120\Omega}{\sqrt{\text{Dk}}} \ln\left(\frac{s}{D} + \sqrt{\left(\frac{s}{D}\right)^2 - 1} \right)$$

Where
Zdiff = the differential impedance
Dk = the effective dielectric constant in the x-y plane
s = the center to center spacing of the round rods (mils)
D = the diameter of the rods (mils)

This model is illustrated in Figure 19.

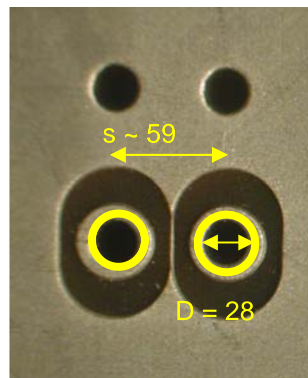


Figure 19. The twin rod model can be applied to the differential via to estimate the differential impedance based on geometry features in the fabricated structure.

Using values for these parameters based on the specific geometry and a Dk value of 6.4, the estimated differential impedance is

$$Zdiff = \frac{120\Omega}{\sqrt{6.4}} \ln\left(\frac{59}{28} + \sqrt{\left(\frac{59}{28}\right)^2 - 1} \right) = 65\Omega$$

This estimated impedance is remarkably close to the extracted differential impedance of 64 ohms.

This analysis suggests the differential impedance of the two vias can be approximated as two round rods. This tight coupling between the vias strongly dominates the differential impedance. Changing the return path design, such as increasing the anti pad clearance holes any further in the planes may have very limited impact on increasing the differential impedance. 3D modeling is needed to quantify this impact and is part of the follow on study.

The dominant terms to increase the differential impedance would be to reduce the via diameter or increase their spacing. Unfortunately, these are difficult to do because they are selected based on compatibility with a specific connector footprint design.

In general, using nominal values for a via design, its differential impedance will be on the low side. However, a low impedance for a differential via, with no via stub, can still be a transparent via to very high bandwidth. To further increase its impedance, bringing it closer to 100 ohms, features could be optimzied, such as removing non functional pads on inner layers and use the largest possible clearance holes in the planes.

Conclusion

This analysis suggests that a really simple model for a differential via transition, consisting of a uniform differential pair, can be used to accurately describe a real differential via to very high bandwidth. The relative length of the thru and stub sections can be easily adjusted in the model.

Due to the anisotropic nature of the dielectric material, the effective dielectric constant the via sees in the x-y direction, is typically higher than the dielectric constant in the z direction. A value of 6.4 was found to be in excellent agreement with the measurements. However, at this point, it is not possible to distinguish between a higher dielectric constant and a distributed capacitive loading from coupling to the planes. The only way to distinguish these two effects is with a 3D field solver.

As illustrated, a simple twin rod model can be used to predict the differential impedance of two coupled signal vias. This model can be used to recommend design features to optimize the performance of vias. The most important parameter is the length of the via stub. Once this is minimized, a second order factor is the impedance of the via pair. In general, the differential impedance will be lower than 100 ohms, so design knobs should be tweaked to try to raise this impedance, However, even with an impedance on the order of 64 ohms, very long vias can be nearly transparent.

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